	Type	L #	Hits	Search Text	DBs
1	BRS	L1	14	(sac or ((self-aligned or self-alignment) adj2 contact)) same (bottom adj2 electrode)	USPAT
2	BRS	L2	101	(sac or ((self-aligned or self-alignment) adj2 contact)) and (bottom adj2 electrode)	USPAT
3	BRS	L3	87	2 not 1	USPAT
4	BRS	L4	797	(sac or ((self-aligned or self-alignment) adj2 contact)) and capacitor	USPAT
5	BRS	L5	727	4 not 2	USPAT
6	BRS	L6	464	((sac or ((self-aligned or self-alignment) adj2 contact)) and dram) not (((sac or ((self-aligned or self-alignment) adj2 contact)) same dram) or ((feram or (ferroelectric near2 ram))))	USPAT
7	BRS	L7	471	5 not 6	USPAT
8	BRS	L8	1517	(sac or ((self-aligned or self-alignment) adj2 contact)) and electrode	USPAT
9	IS&R	L9	377	(438/239).CCLS.	USPAT
10	BRS	L10	362	9 not 7	USPAT
11	IS&R	L11	490	(438/240).CCLS.	USPAT
12	BRS	L12	413	11 not (9 or 7)	USPAT

	Type	L #	Hits	Search Text	DBs
1	BRS	L1	249	(sac or ((self-aligned or self-alignment) adj2 contact)) same dram	USPAT
2	BRS	L2	64	1 same (spacers or spacer)	USPAT
3	BRS	L3	6	(sac or ((self-aligned or self-alignment) adj2 contact)) and (feram or (ferroelectric near2 ram))	USPAT
4	BRS	L4	338	(feram or (ferroelectric near2 ram))	USPAT
5	BRS	L5	29	4 and (spacers or spacer)	USPAT
6	BRS	L6	309	4 not (2 or 5)	USPAT
7	BRS	L7	717	(sac or ((self-aligned or self-alignment) adj2 contact)) and dram	USPAT
8	BRS	L8	462	7 not (1 or 4)	USPAT
9	BRS	L9	3	6211034.URPN.	USPAT
10	BRS	L10	12	("5024722" | "5156992" | "5173442" | "5264076" | "5302547" | "5418388" | "5468342" | "5530279" | "5562801" | "5633210" | "5793076" | "5930639").PN.	USPAT
11	BRS	L11	0	(upper adj2 electrode) near5 ("in" near3 (hole or opening))	USPAT
12	BRS	L12	1	("in" near3 (hole or opening))	USPAT

SUPREME COURT OF THE UNITED STATES

No. 00–1543

FESTO CORPORATION, PETITIONER *v.* SHOKETSU KINZOKU KOG

DOCUMENT-IDENTIFIER: US 6384440 B1
TITLE: Ferroelectric memory including ferroelectric capacitor, one of whose
electrodes is connected to metal silicide film

---------- KWIC ---------

BSPR:
The **bottom electrode is desirably formed of platinum**. The ferroelectric film
formed on a platinum film have excellent characteristics.

CLPR:
11. A ferroelectric memory according to claim 1, wherein said **bottom electrode**
is formed of platinum.

DOCUMENT-IDENTIFIER: US 6169304 B1
TITLE: Semiconductor device having a passivation layer which minimizes diffusion of hydrogen into a dielectric layer

---------- KWIC ---------

DEPR:
On the silicon substrate 31, an insulating layer 37 composed of silicon oxide layer is formed, and a capacitor 41 comprising a **bottom electrode 38 of platinum layer and titanium** layer, a capacitor dielectric layer 39 composed of
ferroelectric layer or high dielectric layer, and a top electrode 40 composed of platinum layer and titanium layer is formed on the insulating layer 37. Covering this capacitor 41, an interlayer insulating layer 42 composed of a PSG
layer having the moisture content of 0.5 g or less per 1 cm.sup.3 is formed. In the conventional semiconductor device having capacitor, the moisture content
of the interlayer insulating layer was 0.9 g or more per 1 cm.sup.3.

DOCUMENT-IDENTIFIER: US 5759903 A
TITLE: Circuit structure having at least one capacitor and a method for the manufacture thereof

---------- KWIC ---------

BSPR:
It is with the frame work of the present invention to employ **silicon dioxide, silicon nitride or titanium dioxide or combinations of these layers as a dielectric layer**. Silicon dioxide is one of the best known dielectrics and can therefore be governed extremely well. Higher capacitances are achieved with a
dielectric of titanium dioxide because of the higher dielectric constant. Especially low defect densities are achieved by using a multi-layer dielectric having a layer sequence of SiO.sub.2, Si.sub.3 N.sub.4, SiO.sub.2.

DOCUMENT-IDENTIFIER: US 6358800 B1
TITLE: Method of forming a MOSFET with a recessed-gate having a channel length
beyond photolithography limit

---------- KWIC ---------

DEPR:
The shallow trench isolation regions 112 are formed by first forming shallow trenches in the semiconductor substrate 110 using the conventional photolithographic and anisotropic reactive ion etching (RIE) procedures. After
removal of the photoresist shape used to define the shallow trenches, a silicon
oxide layer is deposited by low pressure chemical vapor deposition (LPCVD) or
plasma enhanced chemical vapor deposition (PECVD) procedures for completely
filling the shallow trenches. A chemical mechanical polishing (CMP) process is
then performed to remove silicon oxide from the top surface of the semiconductor substrate 110. The first dielectric layer 114 is formed by conventional deposition process such as PECVD or LPCVD to a thickness between
50 to 200 Angstroms. The first **dielectric layer 114 is composed of silicon
dioxide (SiO.sub.2), TiO.sub.2,** Ta.sub.2 O.sub.5 and the like. The second dielectric layer 116 is composed of silicon nitride or silicon oxynitride, and deposited by a low-pressure CVD (LPCVD) process or a plasma-enhanced CVD (PECVD) process to a thickness between 1000 to 2000 Angstroms. The first
dielectric layer and the second dielectric layer should have selective etchability.

DOCUMENT-IDENTIFIER: US 6153460 A
TITLE: Method of fabricating semiconductor memory device

---------- KWIC ---------

DEPR:
Next, as shown in FIG. 2(d), a second insulating film comprising a SiO.sub.2 film 16 is formed on the TiO.sub.2 film 7 inclusive of the node electrode 18, and each opening is formed at a position, over the node electrode 18, that corresponds to the drive line of the capacitor. An about 200 to about 1,000 .ANG.-thick TiO.sub.2 film is deposited onto this opening and is etched back in
order to form a side wall spacer of the TiO.sub.2 film 17 on the side wall of
the SiO.sub.2 film 16.

CLPR:
5. A method of fabricating a semiconductor memory device according to claim 2,
wherein said side wall spacer is made of TiO.sub.2 or TaO.sub.2.

DOCUMENT-IDENTIFIER: US 5638319 A
TITLE: Non-volatile random access memory and fabrication method thereof

---------- KWIC ---------

DEPR:
More specifically, (a) where the bottom electrode, the ferroelectric film and
top electrode have the same configuration with the edges thereof aligned, and
an SiO.sub.2 film, NSG film, BPSG film or the like is formed to cover the top
electrode as an interlayer insulation film; or (b) where the bottom electrode
and the ferroelectric film have the same configuration with the edges thereof
aligned, and the top electrode covers part of the ferroelectric film; and an
SiO.sub.2 film, NSG film, BPSG film or the like is formed to cover the top
electrode as an interlayer insulation film, portions of the ferroelectric film
appearing on the side faces of the ferroelectric capacitor would directly
contact the SiO.sub.2 film or the like. In these cases, lamination of a
diffusion prevention film and a thin insulation film (respectively
corresponding to a TiO.sub.2 film and an SiO.sub.2 film in FIG. 1) or a spacer
of a diffusion prevention film (corresponding to a **spacer of TiO.sub.2** in
FIG.
8) is preferably provided on the side faces of the ferroelectric capacitor.

DEPR:
(e) Where the top electrode is formed on the ferroelectric film covering the
bottom electrode, and the ferroelectric film and the top electrode have the
same configuration with the edges thereof aligned, and an SiO.sub.2 film, NSG
film, BPSG film or the like is formed over the capacitor and below the

capacitor as interlayer insulation films, portions of the ferroelectric film appearing on the side faces and bottom face of the ferroelectric capacitor would directly contact the overlying SiO.sub.2 film and the underlying SiO.sub.2 film or the like. In these cases, a spacer of a diffusion prevention film (corresponding to a spacer of TiO.sub.2 film) is preferably provided on the side faces of the ferroelectric capacitor, and a diffusion prevention film
is preferably provided on the interlayer insulation film (corresponding to TiO.sub.2 film in FIG. 8), on which diffusion prevention film is formed the ferroelectric capacitor.

DEPR:
To ameliorate the degradation in the polarization characteristics of the ferroelectric capacitor which would occur where the SiO.sub.2 film 32 is used
as an interlayer insulation film to be formed on the ferroelectric capacitor as
in Example 2, a non-volatile RAM as shown in FIG. 8 is proposed. The non-volatile RAM cell has substantially the same construction as that in Example 2, except that a spacer 31 is formed of TiO.sub.2 on the side walls of
a capacitor ferroelectric film 18 and top electrode 21 of a ferroelectric capacitor.

DOCUMENT-IDENTIFIER: US 6388281 B1
TITLE: Triple metal line 1T/1C ferroelectric memory device and method for fabrication thereof

---------- KWIC ---------

CLPR:
9. The device according to claim 8, wherein the lower layer of the **upper electrode is made from iridium dioxide** (IrO.sub.2).

DOCUMENT-IDENTIFIER: US 6388281 B1
TITLE: Triple metal line 1T/1C ferroelectric memory device and method for fabrication thereof

---------- KWIC ---------

DEPR:
The lower electrode layer 120 is preferably made from **iridium dioxide (IrO2)**
and the lower electrode layer 122 is preferably made from platinum (Pt). The
iridium dioxide (IrO2) 120 is deposited to a thickness of about 500 angstroms
by a direct current (DC) magnetron sputtering technique. After depositing, high temperature annealing is carried out in an ambient oxygen atmosphere at a
temperature of about 600 degrees C. for the purpose of forming stable oxide
electrode formations. The lower electrode layer 122 of platinum (Pt) is deposited to a thickness of about 1,000 angstroms by a sputtering technique.
The platinum (Pt) lower electrode layer 122 exhibits a crystalline structure, which is preferable to the crystallization of the later-formed ferroelectric film.

CLPR:
6. The device according to claim 5, wherein the lower layer of the lower **electrode is made from iridium dioxide** (IrO.sub.2).

CLPR:
9. The device according to claim 8, wherein the lower layer of the upper **electrode is made from iridium dioxide** (IrO.sub.2).